❑ MN101E32 Series

Type	MN101EF32D
Internal ROM type	FLASH
ROM (byte)	64K+8K
RAM (byte)	4K
Package (Lead-free)	LQFP064-P-1414
Minimum Instruction Execution Time	50 ns (at 2.7 V to 5.5 V, 20 MHz) *: at internal 2 , 3 , 4 , 5 , 6 , 8 , 10 times oscillation used

■ Interrupts

6 external interrupts. 23 internal interrupts

RESET. NMI. External 0 to 4. Timer 0 to 4. Timer 6. Timer 7 (2 systems). Timer 8 (2 systems). Time base. Serial 0 (2 systems). Serial 1 (2 systems). Serial 2 (2 systems). Serial 4. Serial 5. A/D conversion. ATC. Key interrupt

■ Timer Counter

8-bit timer × 7

- Timer 0 .....Timer pulse output. Event count. Added pulse (2-bit) type PWM output. Remote control carrier output. Simple pulse width measurement. Real time output control
- Timer 1 .....Timer pulse output. Event count. 16-bit cascade connected (timer 0, 1). Timer synchronous output
- Timer 2 .....Timer pulse output. Event count. Added pulse (2-bit) type PWM output. Simple pulse width measurement. 24-bit cascade connected (timer 0, 1, 2). Timer synchronous output. Real time output control
- Timer 3 .....Timer pulse output. Event count. Remote control carrier output. 16-bit cascade connected (timer 2, 3). 32-bit cascade connected (timer 0, 1, 2, 3)
- Timer 4 .....Timer pulse output. Added pulse (2-bit) type PWM output. Event count. Serial transfer clock output. Simple pulse width measurement
- Timer 6 .....8-bit freerun timer. Time base timer
- Timer A.....Event count. Baud rate timer. Clock output for peripheral function

16-bit timer × 2

- Timer 7 .....Timer pulse output. Event count. High accuracy PWM. High performance IGBT output (cycle/duty continuous variable). Timer synchronous output. Input capture (both edge available). Real time output control. Double buffer compare register
- Timer 8 .....Timer pulse output. Event count. High accuracy PWM output (cycle/duty continuous variable). Pulse width measurement. Input capture (both edge available). 32-bit cascade connected (timer 7, 8). 32-bit PWM output. Synchronous output event. Double buffer compare register

Watchdog timer × 1

■ Serial interface

Synchronous type/UART (full-duplex) × 3: Serial 0 to 2

Synchronous type/Multi-master I^2C × 1: Serial 4

I^2C slave × 1: Serial 5

■ DMA controller

1 systems. Maximum transfer cycles are 255

Starting factor: External request. Internal event. Software

■ I/O Pins

I/O 54 : Common use. Specified pull-up/pull-down resistor available. Input/output selectable (bit unit)

■ A/D converter

10-bit × 8 channels

■ Display control function

LCD: 32 segments × 4 commons (Static, 1/2, 1/3, or 1/4 duty) 1/3 bias

Usable if VLC1 ≤ VDD

■ Special Ports

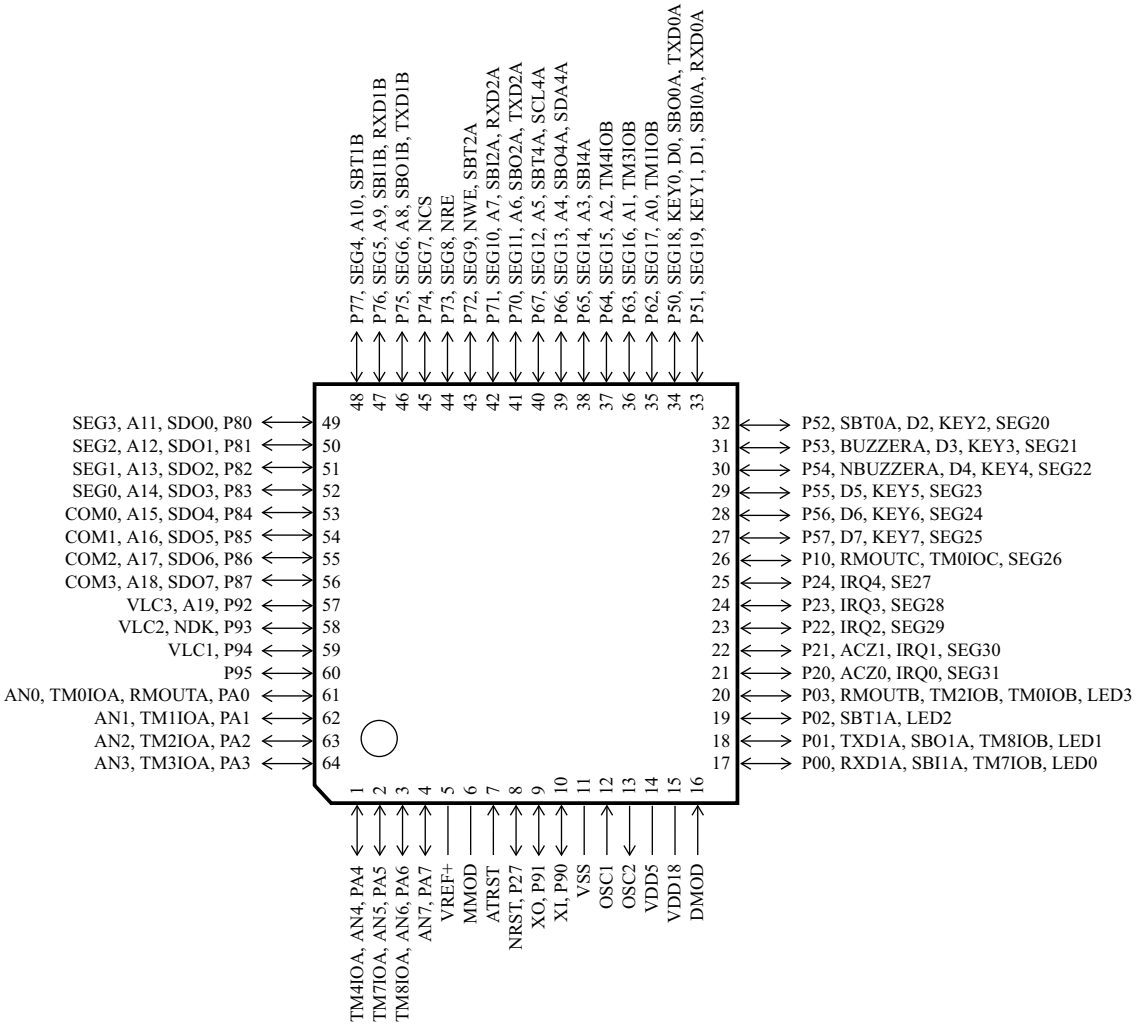
Buzzer output. Inverted buzzer output. Remote control carrier output. High-current drive port

■ ROM Correction

Correcting address designation: Up to 7 addresses possible

■ Pin Assignment

LQFP064-P-1414



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